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[Search Patents](#)**Patents**Patents **11 - 20** on **sampling edge random**. (0.03 seconds)▸ **List view**[Cover view](#)▸ **Sort by relevance**[Sort by date \(new first\)](#)[Sort by date \(old first\)](#)▸ **Any status**[Issued patents](#)[Applications](#)Method and apparatus for receiving synchronous data

US Pat. 6424684 - Filed Aug 30, 1999 - Micron Technology, Inc.

Synchronous Dynamic **Random** Access Memory (hereinafter "SDRAM") is a generic name... The **sampling edge** of the system clock used to read the synchronous data ...Apparatus for random repetitive sampling

US Pat. 4694244 - Filed Feb 21, 1986 - Hewlett Packard Company

SAMPLING FIG. is a block diagram of the synchronizer shown in FIG. ... waveform on each leading **edge** of a sample clock signal In **random** repetitive **sampling**, ...High-speed, two-port dynamic random access memory (DRAM) with a late-write ...

US Pat. 7002868 - Filed Oct 22, 2003 - NEC Electronics Corporation

... at the rising **edge** of the internal clock signal K, a latch circuit 329 for **sampling** the output signal of the latch circuit 50 320 at the falling **edge** of

...

Method and apparatus for correcting for random coincidences in a nuclear ...

US Pat. 5998793 - Filed Apr 17, 1998 - ADAC Laboratories

... because the inner **edge** of the transmission fan beam 38 extends beyond the ... then the **sampling** at the outer **edge** of the transaxial FOV of a detector ...Bootstrap method for writing servo tracks on a disk drive

US Pat. 5541784 - Filed Nov 21, 1994 - Daniel F. Cribbs

... of signal read by the slider at each corresponding **sampling** point; ... large magnitude **random** electrical noise events and/or 55 large magnitude **random** ...Random sampling with phase measurement

US Pat. 6564160 - Filed Jun 22, 2001 - Agilent Technologies, Inc.

The optical **sampling** A sampler strobe 36, when used as an oscilloscope trigger . . . , . . . , r 11 for eye diagrams, is free-running (**random sampling**). ...Method and apparatus for generating random numbers

US Pat. 6480072 - Filed Apr 18, 2000 - Advanced Micro Devices, Inc.

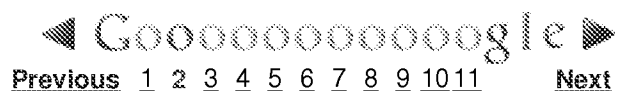
As long as the VCO output reducing the amount of non-**random** information. The ran - frequency is made to vary significantly during the **sampling** domness of 64 ...Acquisition of highly variable data frequency by digital edge processing

US Pat. 6118745 - Filed Jan 26, 1998 - International Business Machines Corporation

Random access is important, for example, in interactive games or for non-sequential ... An **edge** pattern identifier is coupled to the **sampling** detector for ...Timing phase synchronization detecting circuit and demodulator

US Pat. 6097766 - Filed Oct 22, 1998 - Mitsubishi Denki Kabushiki Kaisha

21 22 10 baseband phase data sampled at the rising **edae** of the recovered ...



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Patents

 Patents **1 - 10** on **master slave flip flop**. (0.07 seconds)

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MASTER SLAVE FLIP-FLOP

Master-slave flip-flop circuit with three phase clocking

US Pat. 4843254 - Filed Feb 29, 1988 - Oki Electric Industry Co., Ltd.

 1 2 clock signal and the second clock signal, the first clock **MASTER-SLAVE FLIP-FLOP** CIRCUIT WITH signal being inverter and said another inverter delayed ...

Multiple input master/slave flip flop apparatus

US Pat. 4390987 - Filed Jul 14, 1981 - Rockwell International Corporation

 MULTIPLE INPUT **MASTER/SLAVE FLIP FLOP** APPARATUS INVENTION 5 The present

invention is generally related to electronics and more specifically related to

...

Gate array device having macro cells for forming master and slave cells of ...

US Pat. 4933576 - Filed May 9, 1989 - Fujitsu Limited

 ... where each of the first macro cells include a minimum number of elements for forming a **master** part of a **master-slave flip-flop** circuit and each of the ...

Easily and quickly testable master-slave flipflop circuit

US Pat. 5105100 - Filed Jul 1, 1991 - NEC Corporation

 6, if all of the **master/slave flip-** flops included in the sequential circuits

SLi and SL^are 55 constructed in accordance with the above mentioned ...

HIGH SPEED MASTER-SLAVE FLIP-FLOP

US Pat. 3728561 - Filed Jan 12, 1972

 Both the **master** and the **slave flip-** flops are provided with a transistor gate circuit, the **master flip-flop** being directly connected to the gate circuit ...

Master-slave flip-flop circuit

US Pat. 5001361 - Filed May 9, 1989 - Fujitsu Limited

 On the other hand, the **master-slave flip-flop** circuit is BACKGROUND OF THE INVENTION used in various digital circuits and is used in a form of an The ...

Frequency divider employing multiple stages of master/slave flip-flops

US Pat. 5172400 - Filed Apr 3, 1991 - Mitsubishi Denki Kabushiki Kaisha

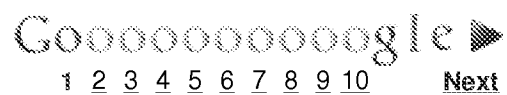
 According to the frequency divider in accordance 10 with the present invention, the 1/N frequency divider is formed using a **master-slave** type **flip-flop** (MS ...

Transistorized master slave flip-flop having threshold offsets generated by ...

US Pat. 4289979 - Filed Aug 28, 1978 - Burroughs Corporation

1 2 the chip and further complicates the fabrication pro- TRANSISTORIZED

MASTER
SLAVE FLIP-FLOP cess. HAVING THRESHOLD OFFSETS GENERATED A third prior art ...



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Patents

 Patents 1 - 10 on **three input xor gate**. (0.06 seconds)

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Exclusive Or/Nor circuit

US Pat. 6469541 - Filed Dec 5, 2001 - Translogic Technology, Inc.

 1 implements a **three- 55 input XOR gate**. Alternatively, output driver 16 may be omitted or configured as a non-inverting driver, in which case circuit 10 ...

Transmitter, receiver, and coding scheme to increase data rate and decrease ...

US Pat. 6851086 - Filed Mar 30, 2001

 The propagation delay between latches is thus attributable to the delay introduced by a 4-**input XOR gate**; an inverter; a **three input AND gate**; and a 2-**input ...**

Programmable shift register

US Pat. 6061417 - Filed Dec 3, 1998 - Xilinx, Inc.

 5, LFSR 500 includes flip-flops 501 through 504, a first **three-input XNOR gate** 510, a second **three-input XNOR gate** 511, a first **three input AND gate** 520, ...

Function block architecture for gate array

US Pat. 6014038 - Filed Mar 21, 1997 - LightSpeed Semiconductor Corporation

 Another example is the five **input XOR gate** shown in FIG. 13. ... A full adder is a function having **three** inputs, A, B, and C, and having two outputs, ...

Pointer for use with a buffer and method of operation

US Pat. 5450560 - Filed Dec 21, 1992 - Motorola, Inc.

 A two-**input AND gate** 112 bit, Ca, as inputs. **XOR gate** 170 has AS and 63 as ... local generate and local propagate func- **Three-input OR gate** 174 receives the ...

Error correction system for n bits using error correcting code designed for ...

US Pat. 5490155 - Filed Oct 2, 1992 - Compaq Computer Corp.

 When the check enable signal is asserted high, the output of the NAND **gate** 160 follows the output of the **three-input XOR gate**, thus transmitting the test ...

Multiplier accumulator circuits

US Pat. 6571268 - Filed Oct 1, 1999 - Texas Instruments Incorporated

 The output from the first two **input XOR gate** 326 is the pi signal 304. ... The first and second **three input AND gates** 320, 322 provide their outputs as the ...

Three input arithmetic logic unit with shifting means at one input forming a ...

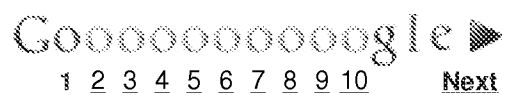
US Pat. 5696954 - Filed Jun 7, 1995 - Texas Instruments Incorporated

 AND **gate** 594 supplies control **input** 20 binations and mixed Boolean and arithmetic ... 9 specify arithmetic logic is formed by **XOR gate** 597, and the bit 16 ...

Fast regular multiplier architecture

US Pat. 6029187 - Filed Oct 28, 1997 - Atmel Corporation

 13 14 10 a sixth logic **gate** consisting of first and second two-**input OR** ... a



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